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Batch: B3

Practical no: EXP-01 (Logic Gate And Half Adder)

1. LOGIC GATE

VHDL CODE :

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity test1 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

C : out STD\_LOGIC);

end test1;

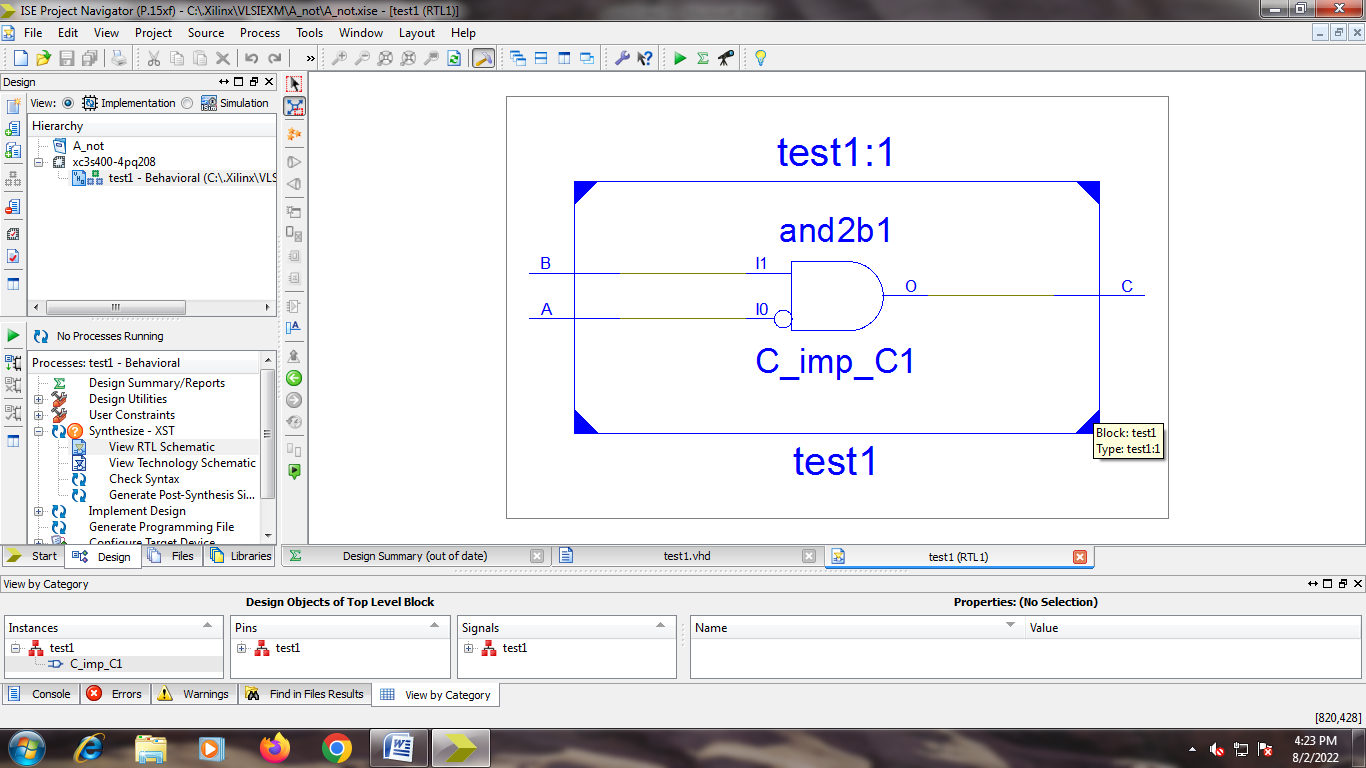
architecture Behavioral of test1 is

begin

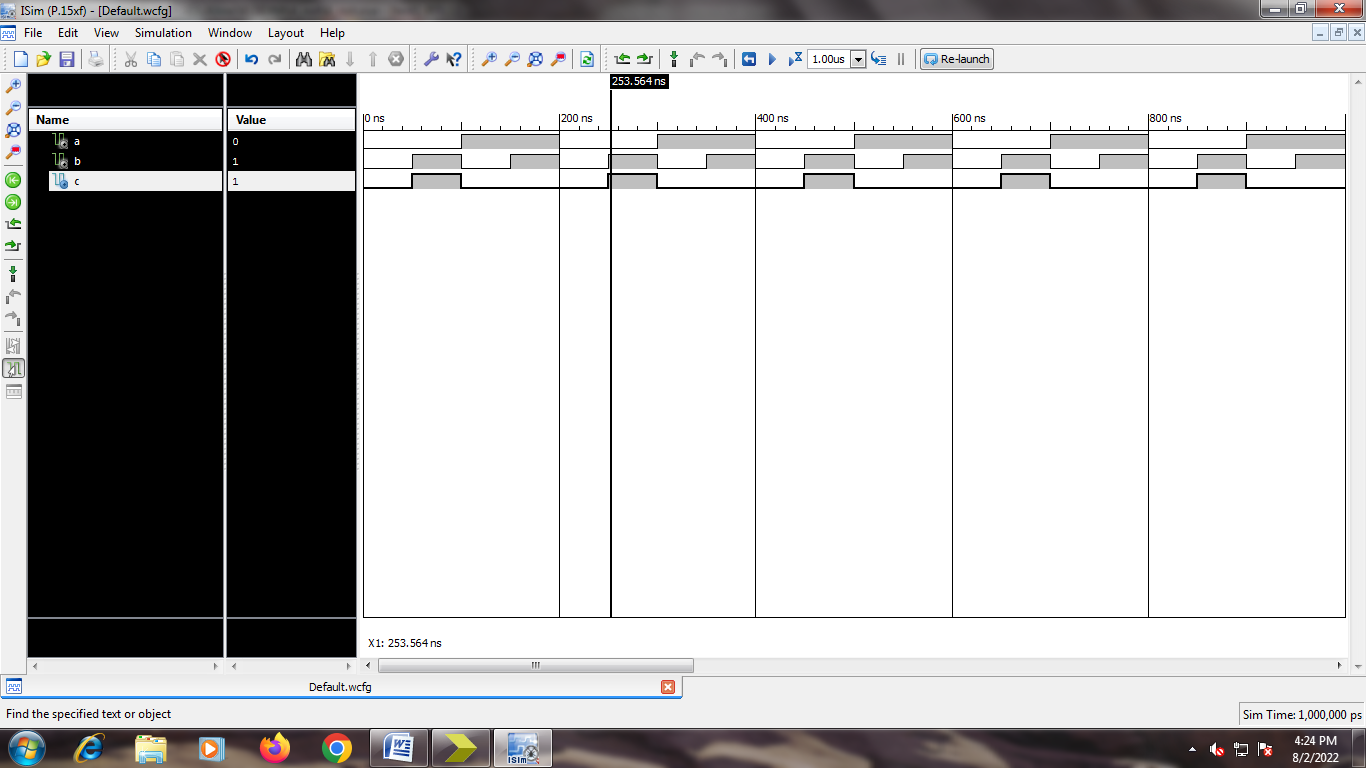
C <= NOT A AND B;

end Behavioral;

RTL :



TEST BENCH:



1. Half ADDER

CODE:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity HAdder is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

S : out STD\_LOGIC;

C : out STD\_LOGIC);

end HAdder;

architecture Behavioral of HAdder is

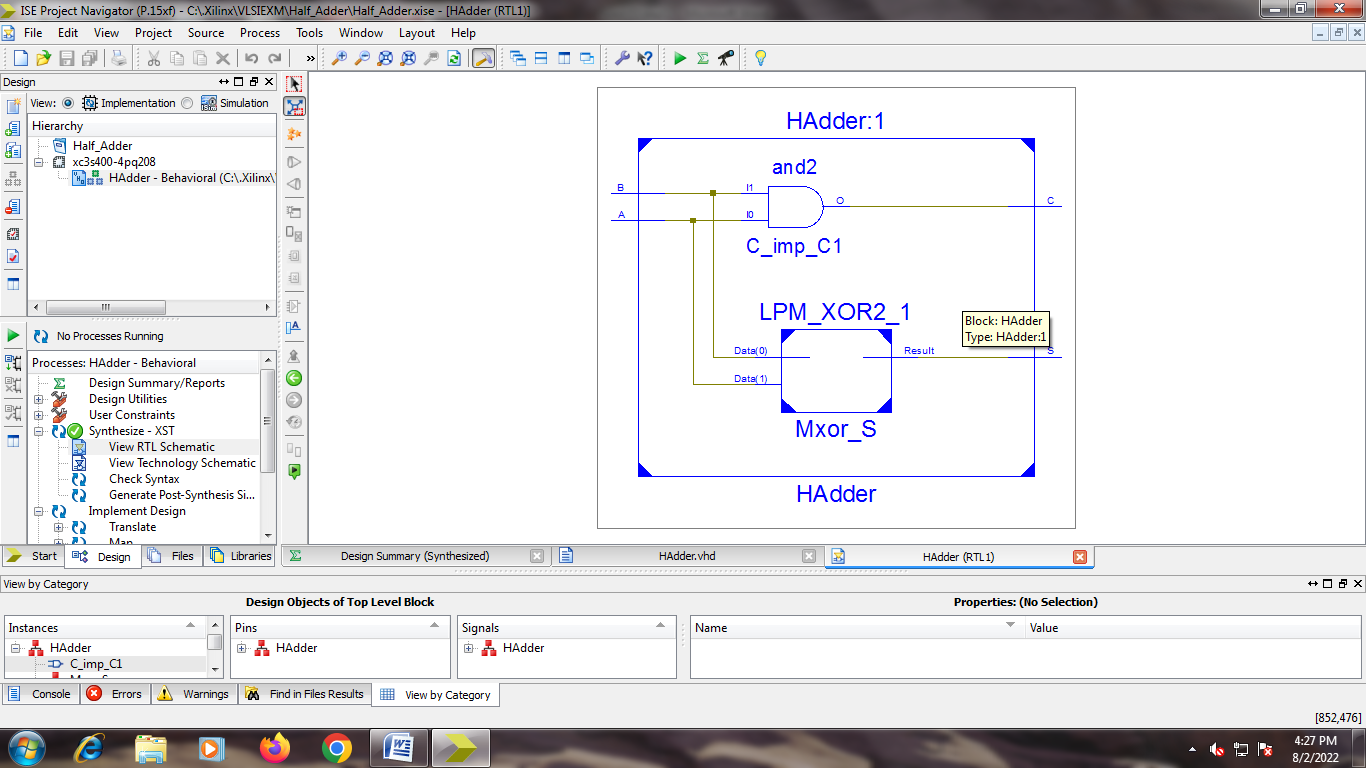
begin

S <= A XOR B;

C <= A AND B;

end Behavioral;

RTL:



Test code:

TEST BENCH:

